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FORM PTO-1390 (REV. 5-93)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		ATTORNEY'S DOCKET NUMBER 10191/2177	
		U.S. APPLICATION NO (If known, see 37 CFR 1.5) <div style="font-size: 1.5em; font-weight: bold; text-align: center;">10/030617</div>	
INTERNATIONAL APPLICATION NO. PCT/DE00/02113		INTERNATIONAL FILING DATE (03.07.00) 03 July 2000	
PRIORITY DATE(S) CLAIMED (03.07.99) 03 July 1999			
TITLE OF INVENTION ELECTRIC SEMICONDUCTOR COMPONENT			
APPLICANT(S) FOR DO/EO/US GOERLACH, Alfred and GEBHARD, Marion			
<p>Applicant(s) herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information</p> <ol style="list-style-type: none"> 1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under <u>35 U.S.C. 371</u>. 2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371 3. <input checked="" type="checkbox"/> This is an express request to begin national examination procedures (35 U.S.C. 371(f)) immediately rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1) 4. <input checked="" type="checkbox"/> A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date. 5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2)) <ol style="list-style-type: none"> a. <input type="checkbox"/> is transmitted herewith (required only if not transmitted by the International Bureau). b. <input checked="" type="checkbox"/> has been transmitted by the International Bureau c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US) 6. <input checked="" type="checkbox"/> A translation of the International Application into English (35 U.S.C. 371(c)(2)) 7. <input checked="" type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)) <ol style="list-style-type: none"> a. <input type="checkbox"/> are transmitted herewith (required only if not transmitted by the International Bureau). b. <input type="checkbox"/> have been transmitted by the International Bureau c. <input type="checkbox"/> have not been made, however, the time limit for making such amendments has NOT expired d. <input checked="" type="checkbox"/> have not been made and will not be made. 8. <input type="checkbox"/> A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)). 9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)) (unsigned) 10. <input type="checkbox"/> A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)). <p>Items 11. to 16. below concern other document(s) or information included:</p> <ol style="list-style-type: none"> 11. <input checked="" type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98 12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included. 13. <input checked="" type="checkbox"/> A FIRST preliminary amendment. <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment 14. <input checked="" type="checkbox"/> A substitute specification and a marked up version thereof. 15. <input type="checkbox"/> A change of power of attorney and/or address letter 16. <input checked="" type="checkbox"/> Other items or information International Search Report, International Preliminary Examination Report and Form PCT/RO/101. 			

Express Mail No. EL244510246

U.S. APPLICATION NO. if known, see 37 C.F.R. 1.5 <div style="font-size: 2em; font-weight: bold;">10/030617</div>		INTERNATIONAL APPLICATION NO PCT/DE00/02113		ATTORNEY'S DOCKET NUMBER 10191/2177	
17. <input checked="" type="checkbox"/> The following fees are submitted.				CALCULATIONS PTO USE ONLY	
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO \$890 00 International preliminary examination fee paid to USPTO (37 CFR 1.482) . . . \$710 00 No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) \$740.00 Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$1,040 00 International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) \$100 00					
ENTER APPROPRIATE BASIC FEE AMOUNT =				\$ 890	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				\$	
Claims	Number Filed	Number Extra	Rate		
Total Claims	10 - 20 =	0	X \$18.00	\$ 0	
Independent Claims	1 - 3 =	0	X \$84.00	\$ 0	
Multiple dependent claim(s) (if applicable)			+ \$280.00	\$ 0	
TOTAL OF ABOVE CALCULATIONS =				\$ 890	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28)				\$	
SUBTOTAL =				\$ 890	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(f))				\$	
TOTAL NATIONAL FEE =				\$ 890	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) \$40.00 per property				\$	
TOTAL FEES ENCLOSED =				\$ 890	
				Amount to be refunded	\$
				charged	\$
a. <input type="checkbox"/> A check in the amount of \$_____ to cover the above fees is enclosed b. <input checked="" type="checkbox"/> Please charge my Deposit Account No. <u>11-0600</u> in the amount of \$890 00 to cover the above fees. A duplicate copy of this sheet is enclosed. c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. <u>11-0600</u> . A duplicate copy of this sheet is enclosed.					
NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.					
SEND ALL CORRESPONDENCE TO <div style="display: flex; justify-content: space-between;"> <div> Kenyon & Kenyon One Broadway New York, New York 10004 CUSTOMER NO. 26646 </div> <div style="text-align: right;"> <div style="font-size: 1.5em; font-family: cursive;">Richard L. Mayer</div> <div style="border-top: 1px solid black; width: 100px; margin-top: -10px;"></div> SIGNATURE </div> </div> <div style="display: flex; justify-content: space-between; margin-top: 20px;"> <div></div> <div style="text-align: right;"> <div style="font-size: 1.5em; font-family: cursive;">January 3, 2002</div> <div style="border-top: 1px solid black; width: 100px; margin-top: -10px;"></div> DATE </div> </div>					

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[10191/2177]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Alfred GOERLACH et al.
Serial No. : To Be Assigned
Filed : Herewith
For : ELECTRIC SEMICONDUCTOR COMPONENT
Art Unit : To Be Assigned
Examiner : To Be Assigned

Assistant Commissioner for Patents
P.O. Box 2327
Arlington, VA 22202

**PRELIMINARY AMENDMENT AND
37 C.F.R. § 1.125 SUBSTITUTE SPECIFICATION STATEMENT**

SIR:

Please amend without prejudice the above-identified application before examination, as set forth below.

IN THE SPECIFICATION AND ABSTRACT:

In accordance with 37 C.F.R. § 1.121(b)(3), a Substitute Specification (including the Abstract, but without claims) accompanies this response. It is respectfully requested that the Substitute Specification (including Abstract) be entered to replace the Specification of record.

IN THE CLAIMS:

On the first page of the claims, first line, change "What is claimed is:" to
--WHAT IS CLAIMED IS:--.

Please cancel, without prejudice, claims 1 to 10 in the underlying PCT application.

81244510246

Please add the following new claims:

- 11. (New) An electric semiconductor component, comprising:
a monocrystalline semiconductor substrate;
an insulation layer arranged on a surface of the semiconductor substrate and
penetrated by at least one contact hole in at least one location; and
a contact structure that contacts the semiconductor substrate through the contact hole
and made of a material in which a semiconductor material of the semiconductor substrate is
soluble in an anisotropic dissolving process;
wherein edges of the contact hole include diffusion stop structures.
12. (New) The semiconductor component according to claim 11, wherein the
diffusion stop structures include curved segments.
13. (New) The semiconductor component according to claim 12, wherein the contact
hole is shaped one of circular and as overlapping intersecting circles.
14. (New) The semiconductor component according to claim 11, wherein the
diffusion stop structures include microstructured sections of the edges.
15. (New) The semiconductor component according to claim 14, wherein the
microstructured sections include one of a crenellated and a sawtooth pattern.
16. (New) The semiconductor component according to claim 15, wherein the one of
the crenellated and the sawtooth pattern includes a plurality of projections, each projection
having an edge length of at most 2 μm .
17. (New) The semiconductor component according to claim 11, wherein the
semiconductor material includes at least one class of crystal planes that is subject to one of
little and no attack in the dissolving process, and the diffusion stop structures include
rectilinear sections of the edges intersecting the crystal planes of the class of crystal planes
extending in the semiconductor substrate beneath the contact hole.

18. (New) The semiconductor component according to claim 11, wherein the contact hole is shaped as one of an equilateral triangle and overlapping, intersecting equilateral triangles.

19. (New) The semiconductor component according to claim 11, wherein the semiconductor substrate includes a $\langle 111 \rangle$ Si substrate.

20. (New) The semiconductor component according to claim 19, wherein the edges of the contact hole are rotated by approximately $\pm 15^\circ$ toward lines of intersection of one of the $\langle 11\bar{1} \rangle$, $\langle 1\bar{1}1 \rangle$ and $\langle \bar{1}11 \rangle$ crystal planes with the surface.--.

REMARKS

This Preliminary Amendment cancels, without prejudice, original claims 1 to 10 in the underlying PCT Application No. PCT/DE00/02113, and adds new claims 11 to 20. The new claims conform the claims to U.S. Patent and Trademark Office rules and do not add new matter to the application.

In accordance with 37 C.F.R. § 1.121(b)(3), the Substitute Specification (including the Abstract, but without the claims) contains no new matter. The amendments reflected in the Substitute Specification (including Abstract) are to conform the Specification and Abstract to U.S. Patent and Trademark Office rules or to correct informalities. As required by 37 C.F.R. § 1.121(b)(3)(iii) and § 1.125(b)(2), a Marked-Up Version of the Substitute Specification comparing the Specification of record and the Substitute Specification also accompanies this Preliminary Amendment. In the Marked-Up Version, underlining indicates added text and bracketing indicated deleted text. Approval and entry of the Substitute Specification (including Abstract) is respectfully requested.

The underlying PCT Application No. PCT/DE00/02113 includes an International Search Report, dated December 8, 2000. The Search Report includes a list of documents that were uncovered in the underlying PCT Application. A copy of the Search Report accompanies this Preliminary Amendment.

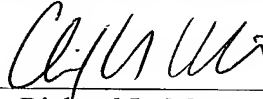
The underlying PCT application also includes an International Preliminary Examination Report, dated September 25, 2001. An English translation of the International Preliminary Examination Report accompanies this Preliminary Amendment.

Applicants assert that the subject matter of the present application is new, non-obvious, and useful. Prompt consideration and allowance of the application are respectfully requested.

Respectfully Submitted,

KENYON & KENYON

Dated: January 3, 2002

By:  (Reg. No. 42,194)
Richard L. Mayer
(Reg. No. 22,490) *for*

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ELECTRIC SEMICONDUCTOR COMPONENT

FIELD OF THE INVENTION

The present invention relates to an electric semiconductor component including a monocrystalline semiconductor substrate, an insulation layer arranged on the surface of the semiconductor substrate and penetrated by a contact hole in at least one location, and a contact element that contacts the semiconductor substrate through the contact hole and is made of a material in which the semiconductor material of the substrate is soluble in an anisotropic dissolving process.

BACKGROUND INFORMATION

Such semiconductor components in which the semiconductor substrate is silicon and the material of the contact element is aluminum are widely used in general. One problem in establishing contact between aluminum and silicon in the area of the contact holes in such components is the solid-state reaction of aluminum with silicon occurring. For a high conductivity of the contact between the two, it is necessary to remove the oxide film which is naturally present between aluminum and silicon in the contact hole. This is accomplished by a temperature treatment in the range of 300°C to 500°C. At these temperatures, metallurgical reactions of aluminum with silicon occur due to the solid-state solubility of each substance in the other at locations where the oxide has been removed. The solubility of silicon in aluminum is on the order of a few percent (e.g., 0.48% at $T = 450^{\circ}\text{C}$), depending on the temperature. The diffusion of silicon in polycrystalline aluminum is very high because of accelerated diffusion along grain boundaries. Therefore, in the course of the temperature treatment, not only is the direct contact hole area saturated with silicon, but also the adjacent aluminum conductor regions become saturated with silicon. Depending on the temperature, a large quantity of silicon may be dissolved away from the

To avoid this problem, it is described D. H. Widmann, H. Mader, H. Friedrich, *Technologie hochintegrierter Schaltungen [Technology of Highly Integrated Circuits]*, Berlin, Springer 1996, for example, that silicon-doped aluminum may be used as the material for the contact structures of electronic components. The silicon concentration of the doped aluminum is greater than the solid-state solubility of silicon in aluminum, based on the highest process temperatures reached in the temperature treatment. This concentration may be approximately 1% silicon.

However, this method cannot be used for contacting in contact holes on high-resistance n-type silicon (donor concentration less than 10^{20} cm^{-3}). Epitaxial silicon deposits are formed in the contact hole area on cooling. These silicon deposits are doped with aluminum and therefore are p-conducting. Because of the formation of the pn junction, they have a negative effect on the contact resistance with increasing degrees of coverage in the contact hole. Therefore, aluminum without added silicon as the metallic coating is used for contacting high-resistance n-type silicon. To produce a conductive junction in the contact hole, the occurrence of spikes must be accepted.

SUMMARY

An object of the present invention is to limit the formation of spikes in a contact hole of a semiconductor component to a great extent by the configuration of the edges of the contact hole. It is not necessary to add additional structures, foreign substances, etc.

There are various configuration possibilities for the edges, which are referred to as diffusion stop structures. Curved segments are the first possibility. For example, a contact hole may be circular as a whole, or it may be composed of overlapping intersecting circles. The effect of the circular segment is based on the fact that it is composed of a plurality of linear segments, each having different directional indices, based on crystalline size dimensions, and that the dissolving process progresses differently along the individual linear segments until reaching the respective areas in the crystalline interior that present the greatest resistance to the dissolving process. The smaller the radius of such a circle, the shorter the corresponding linear segments and also the smaller the spikes that may emanate from a single linear segment.

A similar effect is achieved when the conventional straight bordering lines of a contact hole are replaced by microstructured sections. These microstructured sections may have a crenellated or sawtooth pattern, for example. The dissolving process proceeds regularly from a linear segment of the edge and progresses until reaching sparingly soluble crystal planes. Microstructuring achieves the result that the individual fronts where the dissolving process occurs are shortened in comparison with a rectilinear edge, and that accordingly only a smaller volume of the semiconductor material may be dissolved before reaching planes of the crystal that dissolve only slowly or not at all. The resulting spikes may be shorter as the microstructure becomes finer. An edge length of the structure elements may be 2 μm or less.

However, it is also possible to prevent or at least largely suppress the development of spikes on rectilinear edges of the contact holes. The anisotropy of the dissolving process implies that the semiconductor material has at least one class of crystal planes that are subject to little or no attack in the dissolving process. A class is understood to refer to a family of crystal planes the Miller's indices of which arise from one another through permutation and/or sign reversal. All the planes of such a class are equivalent from a crystallographic standpoint. Rectilinear sections of the edges of a contact hole may be arranged so that they intersect such crystal planes of the class extending beneath the contact hole in the semiconductor substrate.

A contact hole may also be configured so that all its edges fulfill the above-mentioned requirement. Such a contact hole may be in the form of an equilateral triangle or overlapping, intersecting equilateral triangles.

The substrate of the semiconductor component may be a $\langle 111 \rangle$ silicon substrate because the $\langle 111 \rangle$ plane of silicon is hardly subject to attack by dissolving in aluminum.

It is also possible to restrict the formation of spikes on such a substrate by the contact hole having edges that are rotated by $\pm 15^\circ$ toward the lines of intersection of the $\langle 111 \rangle$ plane, the $\langle 1\bar{1}1 \rangle$ plane or the $\langle 11\bar{1} \rangle$ plane with the surface.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of a conventional semiconductor component illustrating the problem of spike formation.

Figure 2 illustrates a surface of a semiconductor substrate having spikes formed at the edge of two contact holes.

Figure 3 is a top view and a sectional view of a semiconductor surface including a contact hole according to an example embodiment of the present invention.

5 Figure 4 illustrates a variant of the contact hole illustrated in Figure 3.

Figure 5 illustrates a semiconductor surface having two circular holes according to an example embodiment of the
10 present invention.

Figure 6 illustrates a variant of the contact holes illustrated in Figure 5.

15 Figure 7 illustrates a semiconductor surface having two contact holes with microstructured edges according to an example embodiment of the present invention.

Figure 8 illustrates two microstructured edges of a contact
20 hole after a temperature treatment.

Figure 9 illustrates a semiconductor surface having edges protected from the formation of spikes due to their orientation relative to planes that are sparingly soluble.
25

DETAILED DESCRIPTION

To illustrate the problem with spikes, Figure 1 is a cross-sectional view through an electronic component including a high-resistance semiconductor substrate 1 and two doped
30 regions 2, 3 formed in it, which are to be separated from one another with a high resistance. An insulation layer 6, which is applied to the surface of the substrate, includes two contact windows 7 through which doped regions 2, 3 are each connected to a contact element 4, 5 made of aluminum of the
35 contact structure. There should not be a conducting connection between contact elements 4, 5. However, during a temperature treatment, which is necessary to produce a satisfactory

electric contact between the doped regions and the contact elements, aluminum diffuses out of contact elements 4, 5 and into semiconductor substrate 1. Since the surface of semiconductor substrate 1 has a $\langle 111 \rangle$ orientation, the aluminum is not able to penetrate far into the depth of the substrate and therefore has spread out parallel to the surface, and spikes 8, 9 have been formed starting from the various contact holes, establishing a conducting junction between regions 2, 3. Therefore, this component is not usable.

Figure 2 illustrates an enlarged detail of a surface of a silicon $\langle 111 \rangle$ wafer 20 including two contact holes 21, 22. Figure 2 does not illustrate the insulation layer at the surface of the wafer, but only shows the insulation layer at the edges of contact holes 21, 22 formed therein. A directional_graphic illustrates projections of the $\langle 111 \rangle$, $\langle 111 \rangle$ and $\langle 111 \rangle$ directions onto the plane of Figure 2. The edges of contact holes 21, 22 which are horizontal in Figure 2 are parallel to a $\langle 110 \rangle$ -oriented flat of wafer 20. The vertical edges of contact holes 21, 22 at the left of Figure 2 show almost no spikes, and the original silicon crystal indicated with hatching extends directly to these edges. At all the other edges, spikes 23 extend far above the original edges of the contact holes to the substrate surface. The reason for this is the orientation of the edges relative to the crystal planes belonging to the same class as the surface. The vertical edges thus extend parallel to the lines of intersection of a crystal face of this class, which may be arbitrarily designated as the $\langle -111 \rangle$ plane. This plane intersects left vertical edges 24, 25 of the two contact holes in an orientation such that it extends beneath the contact holes within the substrate. When in a tempering treatment, an interface between silicon and aluminum propagates slowly perpendicular to the $\langle 111 \rangle$ surface of the other substrate into the depth of the substrate, and a $\langle -111 \rangle$ -oriented interface develops immediately at edges 24, 25 and may also propagate only slowly into the interior of the substrate. However, $\langle 100 \rangle$

interfaces, which present only a low resistance to the dissolving process, are formed at right vertical edges 26, 27, so that spikes 23 are able to propagate there, as well as at the horizontal edges.

5

Figure 3 illustrates a contact hole of a semiconductor component according to a first example embodiment of the present invention, Figure 3a illustrates the contact hole in a top view, and Figure 3b illustrates it in a section along the dash-dot line b-b illustrated in Figure 3a. The semiconductor substrate is a silicon substrate having a $\langle 111 \rangle$ surface. Contact hole 30 develops in the form of an equilateral triangle in an insulation layer 6 on the surface of substrate 1. As indicated by the directional graphic, all three sides extend parallel to the lines of intersection of the surface with crystal planes of the $\langle 111 \rangle$ class. The crystal planes extend through semiconductor substrate 1 beneath the contact hole, as illustrated in Figure 3b on the basis of the example of the $\langle 111 \rangle$ plane. Region 3b in Figure 3b illustrates a zone in which the silicon of semiconductor substrate 1 has penetrated into substrate 1 due to a tempering treatment of a contact made of aluminum attached in contact hole 30. All the interfaces between zone 31 and substrate 1 are class $\langle 111 \rangle$ crystal planes. The lateral propagation of zone 31 over the edges of contact hole 30 is correspondingly small. This propagation is indicated by dotted triangle 32 illustrated in Figure 3a.

It is not crucial for the present invention that contact hole 30 is an exact triangle with acute corners. The corners may also be truncated or rounded, and in this case, interfaces between zone 31 containing aluminum and silicon substrate 1 that do not belong to class $\langle 111 \rangle$ may first be formed on them, unlike the case of a triangle having acute corners, but the final shape that may be achieved by the zone containing aluminum in such a case may correspond to that of triangle 32.

Rectangular contact holes having unequal edge lengths may be desired for contacting semiconductor substrates. Figure 4 illustrates on the basis of a top view of a silicon $\langle 111 \rangle$ substrate having the same orientation as that illustrated in Figure 3, how such a rectangular contact hole indicated by line 40 may be approximated by a plurality of overlapping mutually intersecting equilateral triangles. This yields an elongated contact hole 41 the edges of which form a sawtooth pattern in some areas and in this manner fulfill the requirement at all points that they may intersect crystal planes of class $\langle 111 \rangle$ extending beneath the contact hole in the interior of the substrate.

Figure 5 is a top view of a circular contact hole 50 on a silicon $\langle 111 \rangle$ surface which has exactly the same orientation as that illustrated in Figures 3 and 4. The edge of the contact hole includes three regions 51 that at least approximately fulfill the same condition with regard to their orientation as the edges of the contact holes illustrated in Figures 3 and 4. Accordingly, practically no spikes develop in these regions. In edge areas 52 in between, there are a great many spikes 53, but all of them have only a slight lateral extent. The reason for this is that the circular shape of contact hole 50, based on the size dimension of the crystal lattice, may be regarded as a result of many individual linear segments having different orientations and therefore resisting the dissolving attack of aluminum to different extents, and there is a plurality of lattice sites, e.g., at steps or corners of the interface between the silicon crystal and aluminum, which may function as a seed for the formation of spikes because of their emphasized coordination, or may prevent the propagation of spikes. Therefore, the process of dissolving silicon in aluminum proceeds from a plurality of points in close proximity to one another along the edge and progresses radially outwardly from there, and the crystal faces of the $\langle 111 \rangle$ class, which are not as susceptible to attack, remain. As soon as two spikes have become so deep that

The circular shape of contact hole 50 may be as accurate as possible. For comparison purposes, a second smaller contact hole 54, which is only approximately circular, is also illustrated in Figure 5, its edge being made up of a small number of linear segments. Each linear segment forms the starting point for a spike 53, and since the linear segments are relatively long in comparison with contact hole 50, relatively larger spikes are also formed here.

Figure 6 illustrates a rectangular contact hole that may be approximated by overlapping, intersecting circular contact holes, each having identical diameters r and spacings a_i .

Figure 7 illustrates other example variants of contact holes that are based on the finding that it is appropriate to avoid long, straight edge sections in order to limit propagation of the spikes. Therefore, in the case of contact hole 70, all the edges are crenellated, with small rectangular projections 71 of insulation layer 6 meshing into the interior of the contact hole. Projections 71 have a dimension a parallel to the edge and a dimension b perpendicular to that in the order of $2\text{ }\mu\text{m}$ or less. The period of the crenelation may be $4\text{ }\mu\text{m}$, for example.

As illustrated with respect to contact hole 72, these projections 71 may be omitted on an edge 73, the orientation of which meets the condition defined for the edges of the triangle illustrated in Figure 3.

The effect of projections 71 is illustrated on the basis of Figure 8. The orientation of the semiconductor substrate, more specifically, that of its planes of class $\langle 111 \rangle$, is the same in Figure 8 as in Figures 2 to 7. Figure 8 illustrates the pattern of an edge 80 of a contact element as a solid line.

The edge is richly structured in a plurality of sections, intersecting one another at right angles. During tempering of the component, spikes 81 form along edge 80 and extend beneath the insulation layer until they are only surrounded by
5 interfaces of class $\langle 111 \rangle$ that may be difficult to attack. As illustrated by the comparison of the two edge patterns illustrated in Figure 8, these spikes are more numerous and smaller, the finer the structure of the edge.

10 Figure 9 is a top view of a semiconductor substrate including a plurality of rectangular contact holes 90. The orientation of the semiconductor substrate is the same as that illustrated in the preceding Figures. The edges of the contact holes are rotated by $\pm 15^\circ$ in one of these three directions. This may be
15 the greatest angular deviation from one of the three directions that is possible on a surface having trigonal symmetry like the $\langle 111 \rangle$ surface of silicon. This orientation may guarantee a plurality of exposed points along each edge, from which spikes may form or which prevent the propagation of
20 spikes. Therefore, in tempering the substrate, a large number and density of spikes are formed with aluminum contact elements attached in contact holes 90, but the growth of these spikes may stop in the course of the tempering process as soon as the sparingly soluble interfaces of the spikes begin to
25 come in contact with one another.

Advantages of various embodiments of the present invention have been described above with respect to a silicon $\langle 111 \rangle$ surface and aluminum as the material at the contact elements.

30 It is also possible to apply the present invention to other surfaces, in which case the spikes may then possibly extend into the depth of a substrate rather than parallel to the surface, as well as other combinations of semiconductor material and metal. The semiconductor material may have an
35 anisotropic solubility characteristic with respect to the metal.

ABSTRACT

An electric semiconductor component includes a monocrystalline semiconductor substrate made of silicon, for example, an insulation layer arranged on the surface of the semiconductor substrate and penetrated by a contact hole in at least one location and a contact element that contacts the semiconductor substrate through the contact hole and is made of a material in which the semiconductor material of the substrate is soluble in an anisotropic dissolving process. The edges of the contact hole are configured as diffusion stop structures.

(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES
PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG(19) Weltorganisation für geistiges Eigentum
Internationales Büro(43) Internationales Veröffentlichungsdatum
11. Januar 2001 (11.01.2001)

PCT

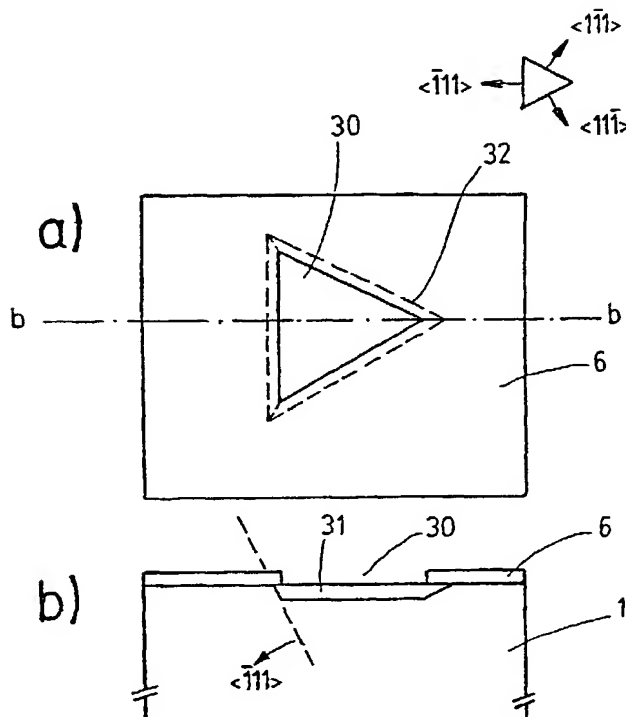
(10) Internationale Veröffentlichungsnummer
WO 01/03195 A1

- (51) Internationale Patentklassifikation⁷: H01L 29/41, 21/28 (71) Anmelder (für alle Bestimmungsstaaten mit Ausnahme von US): ROBERT BOSCH GMBH [DE/DE]; Postfach 30 02 20, D-70442 Stuttgart (DE).
- (21) Internationales Aktenzeichen: PCT/DE00/02113 (72) Erfinder; und (75) Erfinder/Anmelder (nur für US): GOERLACH, Alfred [DE/DE]; Bismarckstrasse 70, D-72127 Kusterdingen (DE). GEBHARD, Marion [DE/DE]; Im Felgenbaechle 10, D-72760 Reutlingen (DE).
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- (25) Einreichungssprache: Deutsch (81) Bestimmungsstaaten (national): JP, US.
- (26) Veröffentlichungssprache: Deutsch (84) Bestimmungsstaaten (regional): europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
- (30) Angaben zur Priorität: 199 30 797.0 3. Juli 1999 (03.07.1999) DE

[Fortsetzung auf der nächsten Seite]

(54) Title: ELECTRIC SEMICONDUCTOR ELEMENT WITH A CONTACT HOLE

(54) Bezeichnung: ELEKTRISCHES HALBLEITERBAUELEMENT MIT EINEM KONTAKTLÖCH



(57) Abstract: An electric semiconductor element comprising a monocrystalline semiconductor substrate which is made, for example, out of silicon; an insulating layer (6) which is penetrated by a contact hole (30) on at least one point and arranged on the surface of the semiconductor substrate (1); in addition to a contact element which comes into contact with the semiconductor substrate (1) by means of the contact hole (30) and which is made of a material such as aluminium, whereby the semiconductor material of the substrate can be dissolved in an anisotropic process. The edges of the contact hole (30) are configured as diffusion-preventing structures.

(57) Zusammenfassung: Ein elektrisches Halbleiterbauelement umfasst ein einkristallines Halbleitersubstrat, zum Beispiel aus Silicium, eine an wenigstens einer Stelle von einem Kontaktloch (30) durchbrochene, an der Oberfläche des Halbleitersubstrats (1) angeordnete Isolationsschicht (6) und ein das Halbleitersubstrat (1) durch das Kontaktloch (30) berührendes Kontaktelement aus einem Material wie zum Beispiel Aluminium, in dem das Halbleitermaterial des Substrats in einem anisotropen Lösevorgang löslich ist. Die Ränder des Kontaktlochs (30) sind als Diffusionsstoppstrukturen ausgebildet.

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ELECTRIC SEMICONDUCTOR COMPONENT

The present invention relates to an electric semiconductor component having a monocrystalline semiconductor substrate, an insulation layer arranged on the surface of the semiconductor substrate and penetrated by a contact hole in at least one location and a contact element which contacts the semiconductor substrate through the contact hole and is made of a material in which the semiconductor material of the substrate is soluble in an anisotropic dissolving process.

Such semiconductor components in which the semiconductor substrate is silicon and the material of the contact element is aluminum are widely used in general. One problem in establishing contact between aluminum and silicon in the area of the contact holes in such components is the solid-state reaction of aluminum with silicon taking place there. For a high conductivity of the contact between the two, it is necessary to remove the oxide film which is naturally always present between aluminum and silicon in the contact hole. This is accomplished by a temperature treatment in the range of 300°C to 500°C. At these temperatures, metallurgical reactions of aluminum with silicon occur due to the solid-state solubility of each substance in the other at locations where the oxide has been removed. The solubility of silicon in aluminum is in the order of a few percent (e.g., 0.48% at T = 450°C), depending on the temperature. The diffusion of silicon in polycrystalline aluminum is very high because of accelerated diffusion along grain boundaries. Therefore, in the course of the temperature treatment, not only is the direct contact hole area saturated with silicon but also the adjacent aluminum conductor regions become saturated with silicon. Depending on the temperature, a large quantity of silicon may be dissolved away from the surface of the semiconductor component and may migrate into the aluminum

contact structure. In a temperature treatment at 450°C for three minutes, for example, the diffusion length of the silicon atoms amounts to approx. 40 μm. The silicon atoms dissolved out of the crystal are replaced by aluminum atoms migrating out of the contact structure. They form "spikes" which are deposits of aluminum having a silicon content. The dimensions of these spikes become larger as the size of the contact hole becomes smaller and the volume of aluminum to be saturated in relation to it becomes larger. These spikes may greatly distort electric fields in the area of the contact hole or may lead to total failure of the component if they extend to a pn junction of the component.

To avoid this problem, it is known from D. H. Widmann, H. Mader, H. Friedrich, *Technologie hochintegrierter Schaltungen* [Technology of Highly Integrated Circuits], Berlin, Springer 1996, for example, that silicon-doped aluminum may be used as the material for the contact structures of electronic components. The silicon concentration of the doped aluminum is greater than the solid-state solubility of silicon in aluminum, based on the highest process temperatures reached in the temperature treatment. This concentration may be approx. 1% silicon.

However, this method cannot be used for contacting in contact holes on high-resistance n-type silicon (donor concentration less than 10^{20} cm^{-3}). Epitaxial silicon deposits are formed in the contact hole area on cooling. These silicon deposits are doped with aluminum and therefore are p-conducting. Because of the formation of the pn junction, they have a negative effect on the contact resistance with increasing degrees of coverage in the contact hole. Therefore, aluminum without added silicon as the metallic coating is used for contacting high-resistance n-type silicon. To produce a conductive junction in the contact hole, the occurrence of spikes must be accepted.

Advantages of the Invention

The present invention is based on the surprising finding that the formation of spikes in a contact hole of a semiconductor component may be limited to a great extent by skillful design of the edges of the contact hole. It is not necessary to add
5 additional structures, foreign substances, etc.

There are various design possibilities for the edges, which are referred to here as diffusion stop structures. Curved segments are the first possibility of this type. For example,
10 a contact hole may be circular as a whole, or it may be composed of overlapping intersecting circles. The effect of the circular segment is based on the fact that it is composed of a plurality of linear segments, each having different directional indices, based on crystalline size dimensions, and
15 that the dissolving process progresses differently along the individual linear segments until reaching the respective areas in the crystalline interior which present the greatest resistance to the dissolving process. The smaller the radius of such a circle, the shorter the corresponding linear
20 segments and also the smaller the spikes which may emanate from a single linear segment.

A similar effect is achieved when the conventional straight bordering lines of a contact hole are replaced by
25 microstructured sections. These microstructured sections may have a crenellated or sawtooth pattern, for example. Here again, the dissolving process proceeds regularly from a linear segment of the edge and progresses until reaching sparingly soluble crystal planes. Microstructuring achieves the result
30 that the individual fronts where the dissolving process takes place are shortened in comparison with a rectilinear edge, and that accordingly only a smaller volume of the semiconductor material may be dissolved before reaching planes of the crystal that dissolve only slowly or not at all. It is true in
35 general that the resulting spikes will be shorter as the microstructure becomes finer. A preferred edge length of the structure elements is 2 μm or less.

However, it is also possible to prevent or at least largely suppress the development of spikes on rectilinear edges of the contact holes. The anisotropy of the dissolving process implies that the semiconductor material has at least one class of crystal planes which are subject to little or no attack in the dissolving process. A class is understood to refer to a family of crystal planes whose Miller's indices arise from one another through permutation and/or sign reversal. All the planes of such a class are equivalent from a crystallographic standpoint. Rectilinear sections of the edges of a contact hole should preferably be arranged so that they intersect such crystal planes of the class running beneath the contact hole in the semiconductor substrate.

A contact hole may also be designed so that all its edges fulfill the above-mentioned requirement. Such a contact hole may be in the form of an equilateral triangle or overlapping, intersecting equilateral triangles.

The substrate of the semiconductor component is preferably a $\langle 111 \rangle$ silicon substrate, because the $\langle 111 \rangle$ plane of silicon is hardly subject to attack by dissolving in aluminum.

It is also possible to restrict the formation of spikes on such a substrate by the fact that the contact hole has edges which are rotated by $\pm 15^\circ$ toward the lines of intersection of the $\langle 11\bar{1} \rangle$ plane, the $\langle 1\bar{1}1 \rangle$ plane or the $\langle \bar{1}11 \rangle$ plane with the surface.

Other features and advantages of the present invention are derived from the following description of exemplary embodiments with reference to the figures.

Figures

Figure 1 shows in a cross section a conventional semiconductor component to illustrate the problem of spike formation;

5 Figure 2 shows a surface of a semiconductor substrate having spikes formed at the edge of two contact holes;

10 Figure 3 shows a semiconductor surface having a contact hole according to the present invention in a top view and in a sectional view;

Figure 4 shows a variant of the contact hole from Figure 3;

15 Figure 5 shows a semiconductor surface having two circular holes according to the present invention;

Figure 6 shows a variant of the contact holes from Figure 5;

20 Figure 7 shows a semiconductor surface having two contact holes having microstructured edges according to the present invention;

25 Figure 8 shows two microstructured edges of a contact hole after a temperature treatment; and

Figure 9 shows a semiconductor surface having edges protected from the formation of spikes due to its orientation relative to planes that are sparingly soluble.

30 Description of the Exemplary Embodiments

To illustrate this problem, Figure 1 shows a section through an electronic component having a high-resistance semiconductor substrate 1 and two doped regions 2, 3 formed in it, which are to be separated from one another with a high resistance. An insulation layer 6 which is applied to the surface of the substrate has two contact windows 7 through which doped

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regions 2, 3 are each connected to a contact element 4, 5 made of aluminum of the contact structure. There should not be a conducting connection between contact elements 4, 5. However, during a temperature treatment, which is necessary to produce a satisfactory electric contact between the doped regions and the contact elements, aluminum diffuses out of contact elements 4, 5 and into semiconductor substrate 1. Since the surface of semiconductor substrate 1 has a $\langle 111 \rangle$ orientation, the aluminum is not able to penetrate far into the depth of the substrate and therefore has spread out in parallel to the surface even more, and spikes 8, 9 have been formed starting from the various contact holes, establishing a conducting junction between regions 2, 3. Therefore, this component is not usable.

Figure 2 shows an enlarged detail of a surface of a silicon $\langle 111 \rangle$ wafer 20 having two contact holes 21, 22. This does not show the insulation layer at the surface of the wafer, only the edges of contact holes 21, 22 formed therein. A directional diagram inserted here shows the projections of the $\langle 11\bar{1} \rangle$, $\langle \bar{1}11 \rangle$ and $\langle \bar{1}\bar{1}1 \rangle$ directions onto the plane of the figure. The edges of contact holes 21, 22 which are horizontal in the figure are parallel to a $\langle 110 \rangle$ -oriented flat of wafer 20. The vertical edges of contact holes 21, 22 at the left of the figure show almost no spikes, and the original silicon crystal shown with hatching extends directly to these edges. At all the other edges, spikes 23 extend far above the original edges of the contact holes to the substrate surface. The reason for this is the orientation of the edges relative to the crystal planes belonging to the same class as the surface. The vertical edges thus run parallel to the lines of intersection of a crystal face of this class which shall be arbitrarily designated as the $\langle -111 \rangle$ plane here. This plane intersects left vertical edges 24, 25 of the two contact holes in an orientation such that it extends beneath the contact holes within the substrate. When in a tempering treatment an interface between silicon and aluminum propagates slowly

perpendicular to the $\langle 111 \rangle$ surface of the other substrate into the depth of the substrate, a $\langle -111 \rangle$ -oriented interface develops immediately at edges 24, 25 and may also propagate only slowly into the interior of the substrate. However, $\langle 100 \rangle$ interfaces, which present only a low resistance to the dissolving process, are formed at right vertical edges 26, 27, so that spikes 23 are able to propagate there, as well as at the horizontal edges.

Figure 3 shows a contact hole of a semiconductor component according to a first embodiment of the present invention, Figure 3a shows the contact hole in a top view, and Figure 3b shows it in a section along the dash-dot line b-b from Figure 3a. The semiconductor substrate is a silicon substrate having a $\langle 111 \rangle$ surface. Contact hole 30 develops in the form of an equilateral triangle in an insulation layer 6 on the surface of substrate 1. As shown by the directional diagram, all three sides run parallel to the lines of intersection of the surface with crystal planes of the $\langle 111 \rangle$ class. The crystal planes run through semiconductor substrate 1 beneath the contact hole, as illustrated in Figure 3b on the basis of the example of the $\langle \bar{1}11 \rangle$ plane. Region 3b in Figure 3b shows a zone in which the silicon of semiconductor substrate 1 has penetrated into substrate 1 due to a tempering treatment of a contact (not shown in this figure) made of aluminum attached in contact hole 30. All the interfaces between zone 31 and substrate 1 are class $\langle 111 \rangle$ crystal planes. The lateral propagation of zone 31 over the edges of contact hole 30 is correspondingly small. This propagation is indicated by dotted triangle 32 in Figure 3a.

It is not crucial for the present invention that contact hole 30 is an exact triangle with acute corners. The corners may also be truncated or rounded, and in this case interfaces between zone 31 containing aluminum and silicon substrate 1 which do not belong to class $\langle 111 \rangle$ might first be formed on them, unlike the ideal case of a triangle having acute

corners, but the final shape that could be achieved by the zone containing aluminum in such a case would also correspond to that of triangle 32.

5 Rectangular contact holes having unequal edge lengths are often desired for contacting semiconductor substrates. Figure 4 shows on the basis of a top view of a silicon $\langle 111 \rangle$ substrate having the same orientation as in Figure 3, how such a rectangular contact hole indicated by line 40 may be
10 approximated by a plurality of overlapping mutually intersecting equilateral triangles. This yields an elongated contact hole 41 whose edges form a sawtooth pattern in some areas and in this way fulfill the requirement at all points that they should intersect crystal planes of class $\langle 111 \rangle$
15 running beneath the contact hole in the interior of the substrate.

Figure 5 shows a top view of a circular contact hole 50 on a silicon $\langle 111 \rangle$ surface which has exactly the same orientation
20 as in Figures. 3 and 4. The edge of the contact hole has three regions 51 which at least approximately fulfill the same condition with regard to their orientation as the edges of the contact holes from Figures. 3 and 4. Accordingly, practically no spikes develop in these regions. In edge areas 52 in
25 between, there are a great many spikes 53, but all of them have only a slight lateral extent. The reason for this is that the circular shape of contact hole 50, based on the size dimension of the crystal lattice, may be regarded as a result of many individual linear segments having different
30 orientations and therefore resisting the dissolving attack of aluminum to different extents, and there is a plurality of lattice sites, e.g., at steps or corners of the interface between the silicon crystal and aluminum, which may function as a seed for the formation of spikes because of their
35 emphasized coordination, or may prevent the propagation of spikes. Therefore, the process of dissolving silicon in aluminum proceeds from a plurality of points in close

proximity to one another along the edge and progresses radially outward from there, and the crystal faces of the $\langle 111 \rangle$ class, which are not as susceptible to attack, remain. As soon as two spikes have become so deep that their bordering faces are in contact, the dissolving process essentially comes to a standstill.

It is important here that the circular shape of contact hole 50 should be as accurate as possible. For comparison purposes, a second smaller contact hole 54 which is only approximately circular is also shown, its edge being made up of a small number of linear segments. Each linear segment here forms the starting point for a spike 53, and since the linear segments are relatively long in comparison with contact hole 50, relatively larger spikes are also formed here.

As shown by Figure 6 in a diagram similar to that in Figure 5, a rectangular contact hole may also be approximated by overlapping, intersecting circular contact holes, each having identical diameters r and spacings a_1 .

Figure 7 shows other variants of contact holes which are also based on the finding that it is appropriate to avoid long, straight edge sections in order to limit propagation of the spikes. Therefore, in the case of contact hole 70, all the edges are crenellated, with small rectangular projections 71 of insulation layer 6 meshing into the interior of the contact hole. Projections 71 have a dimension a parallel to the edge and a dimension b perpendicular to that in the order of $2 \mu\text{m}$ or less each. The period of the crenelation may be $4 \mu\text{m}$, for example.

As shown on the example of contact hole 72, these projections 71 may be omitted on an edge 73 whose orientation meets the condition defined for the edges of the triangle from Figure 3.

The effect of projections 71 is illustrated on the basis of Figure 8. The orientation of the semiconductor substrate, more specifically, that of its planes of class $\langle 111 \rangle$, is the same in this figure as in Figures. 2 through 7. Figure 8 shows the pattern of an edge 80 of a contact element as a solid line. The edge is richly structured in a plurality of sections, intersecting one another at right angles. During tempering of the component, spikes 81 form along edge 80 and extend beneath the insulation layer until they are only surrounded by interfaces of class $\langle 111 \rangle$ which are difficult to attack. As shown by the comparison of the two edge patterns in Figure 8, these spikes are more numerous and smaller, the finer the structure of the edge.

Figure 9 shows a top view of a semiconductor substrate having a plurality of rectangular contact holes 90. The orientation of the semiconductor substrate is the same as that in the preceding figures. The edges of the contact holes here are rotated by $\pm 15^\circ$ in one of these three directions. This is the greatest angular deviation from one of the three directions that is possible at all on a surface having trigonal symmetry like the $\langle 111 \rangle$ surface of silicon. This orientation guarantees a plurality of exposed points along each edge from which spikes may form or which prevent the propagation of spikes. Therefore, in tempering the substrate, a large number and density of spikes are formed with aluminum contact elements attached in contact holes 90, but the growth of these spikes comes to a standstill in the course of the tempering process as soon as the sparingly soluble interfaces of the spikes begin to come in contact with one another.

The main points of the present invention have been described above from the standpoint of a silicon $\langle 111 \rangle$ surface and aluminum as the material at the contact elements. It would be readily conceivable to apply the present invention to other surfaces, in which case the spikes might then possibly extend into the depth of a substrate rather than parallel to the

surface, as well as other combinations of semiconductor material and metal. The only important thing is that the semiconductor material must have an anisotropic solubility characteristic with respect to the metal.

What is claimed is:

1. An electric semiconductor component having a monocrystalline semiconductor substrate (1), an insulation layer (6) arranged on the surface of the semiconductor substrate (1) and penetrated by a contact hole (30, 41, 50, 70) in at least one location, and a contact structure which contacts the semiconductor substrate (1) through the contact hole (6) and is made of a material in which the semiconductor material of the substrate is soluble in an anisotropic dissolving process, wherein the edges of the contact hole (30, 41, 50, 70) are designed as diffusion stop structures.
2. The semiconductor component according to Claim 1, wherein the diffusion stop structures include curved segments.
3. The semiconductor component according to Claim 2, wherein the contact hole (50) is designed to be circular or as overlapping intersecting circles.
4. The semiconductor component according to one of the preceding claims, wherein the diffusion stop structures include microstructured sections of the edges (80).
5. The semiconductor component according to Claim 4, wherein the microstructured sections (80) have a crenellated or sawtooth pattern.
6. The semiconductor component according to Claim 5, wherein the crenelations or sawteeth are formed by projections (71), each having an edge length of 2 μm or less.
7. The semiconductor component according to one of the preceding claims, wherein the material of the semiconductor substrate has at least one class of crystal planes which are subject to little or no attack in the dissolving process; and the diffusion stop structures include rectilinear sections of

[illegible]

the edges intersecting such crystal planes of the class running beneath the contact hole (30, 41) in the semiconductor substrate (1).

8. The semiconductor component according to Claim 8, wherein the contact hole (30, 41) is in the form of an equilateral triangle or overlapping, intersecting equilateral triangles.

9. The semiconductor component according to one of the preceding claims, wherein the substrate is a <111> Si substrate.

10. The semiconductor substrate according to Claim 9, wherein the contact hole has edges which are rotated by approx. $\pm 15^\circ$ toward the lines of intersection of the $\langle 11\bar{1} \rangle$, $\langle 1\bar{1}1 \rangle$ or $\langle \bar{1}11 \rangle$ crystal planes with the surface.

Abstract

An electric semiconductor component includes a monocrystalline semiconductor substrate made of silicon, for example, an
5 insulation layer (6) arranged on the surface of the semiconductor substrate (1) and penetrated by a contact hole (30) in at least one location and a contact element which contacts the semiconductor substrate (1) through the contact hole (30) and is made of a material in which the semiconductor
10 material of the substrate is soluble in an anisotropic dissolving process. The edges of the contact hole (30) are designed as diffusion stop structures.

Fig. 1

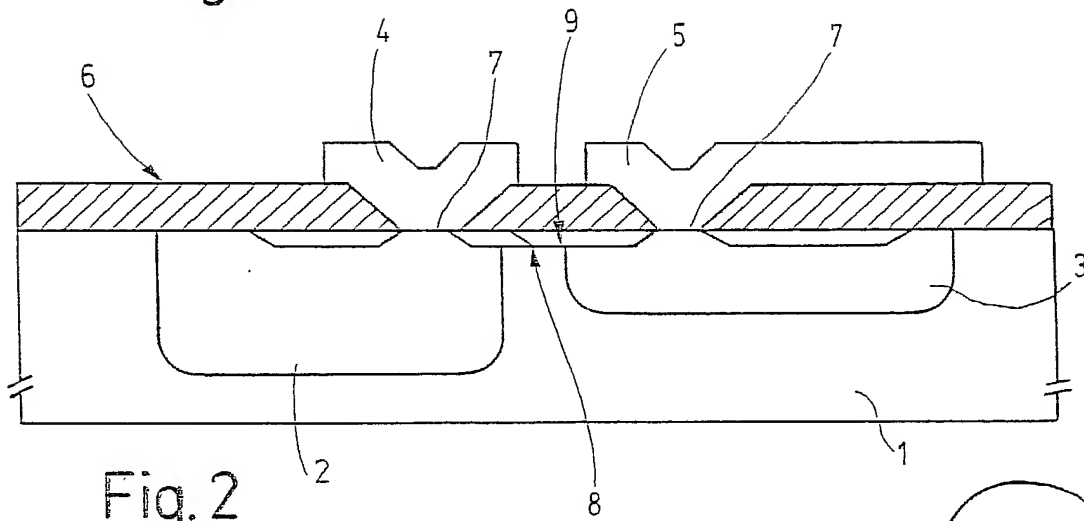


Fig. 2

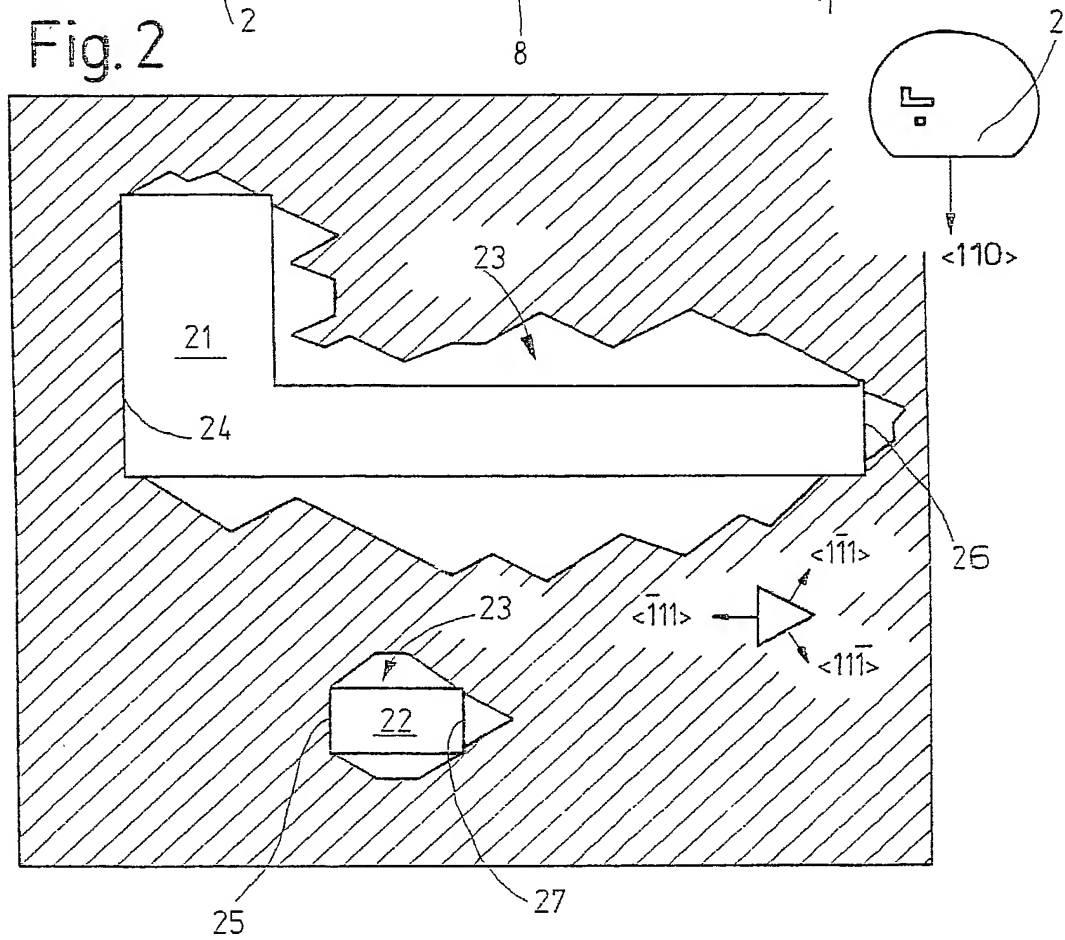


Fig. 3

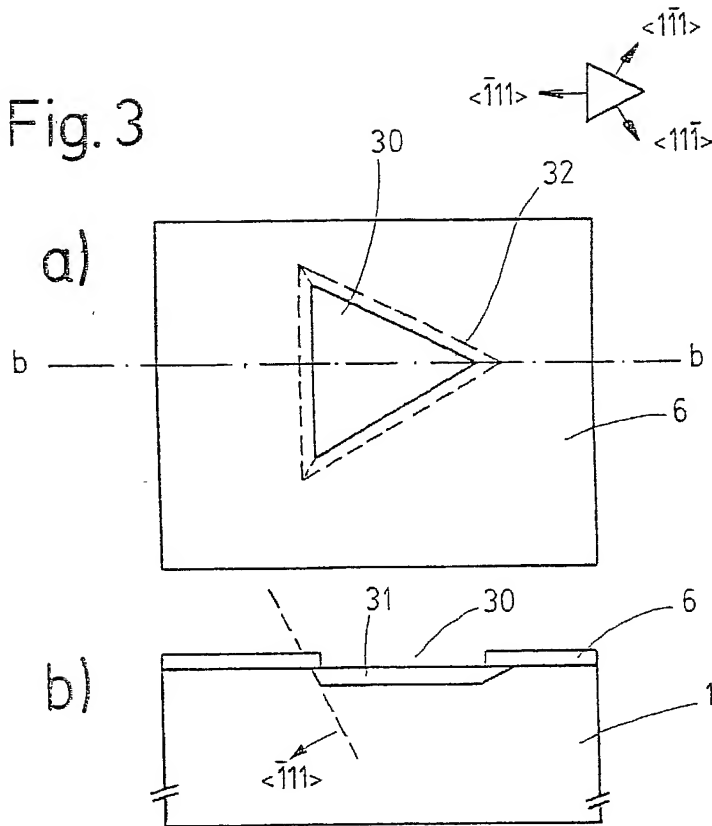


Fig. 4

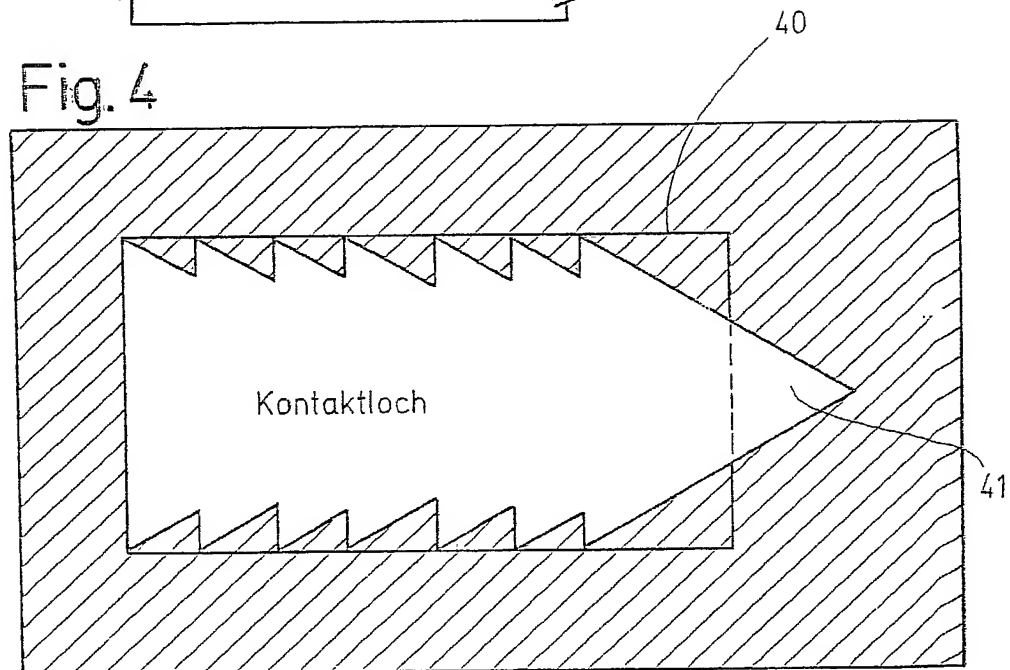


Fig. 5

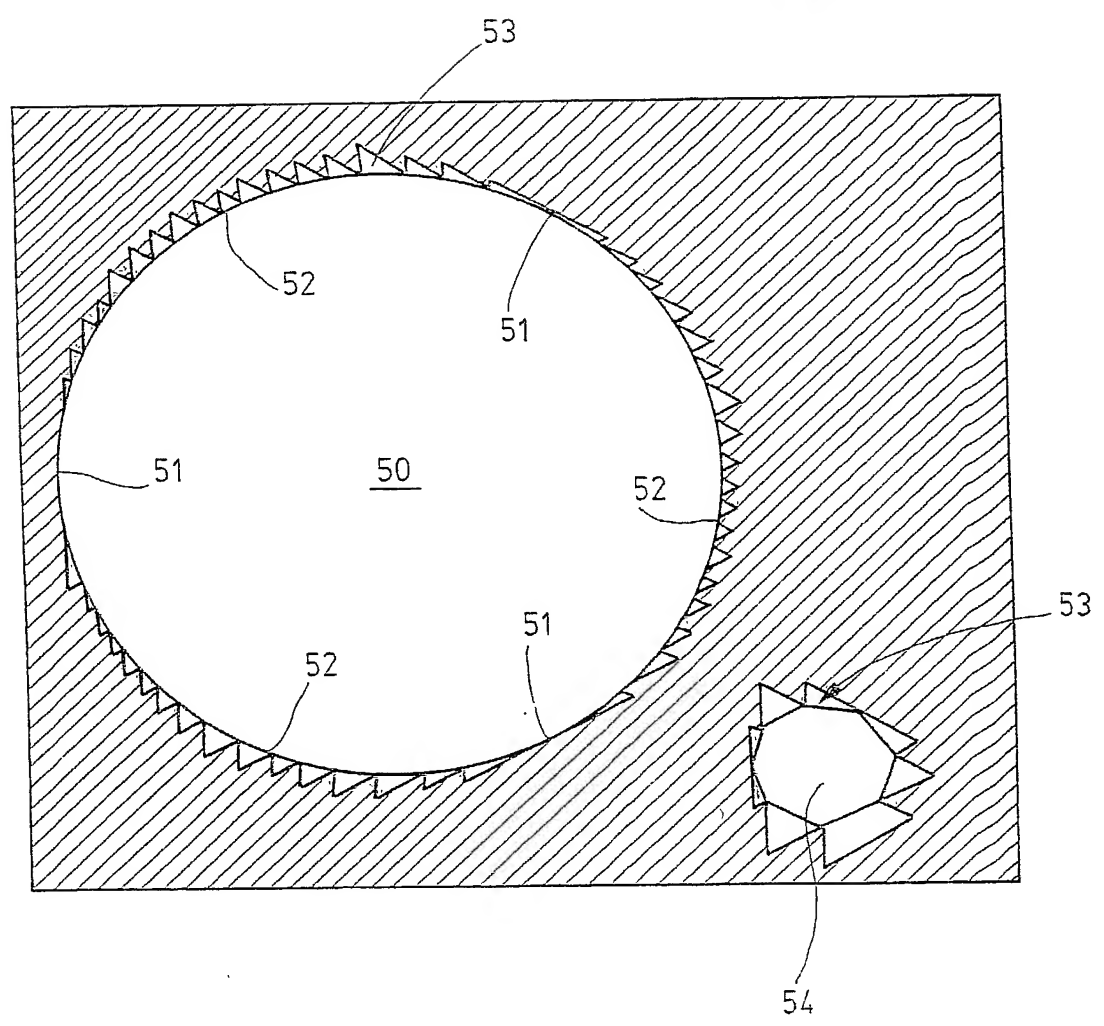
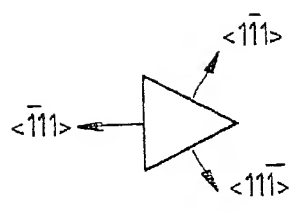


Fig. 6

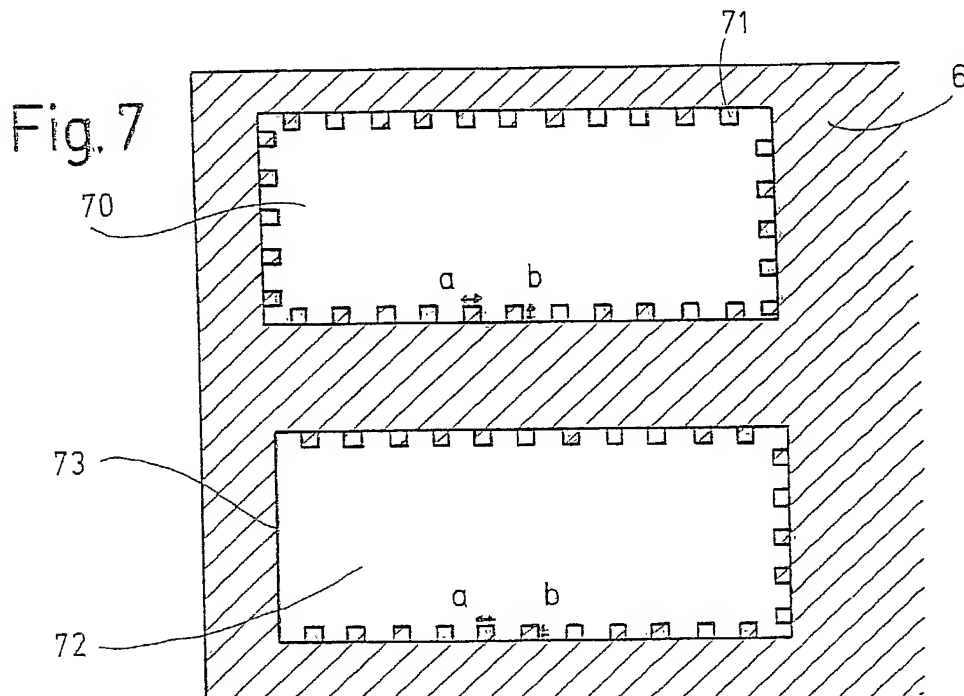
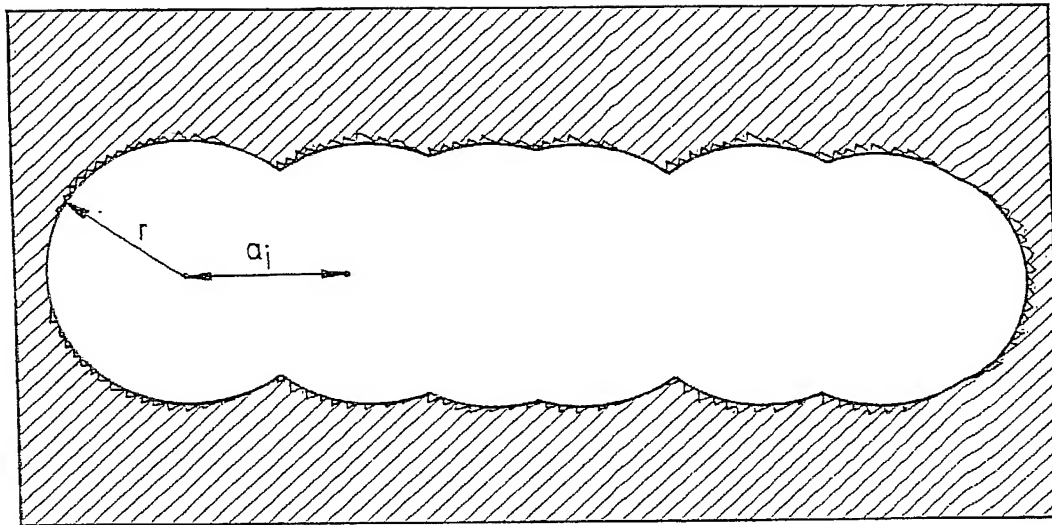


Fig. 8

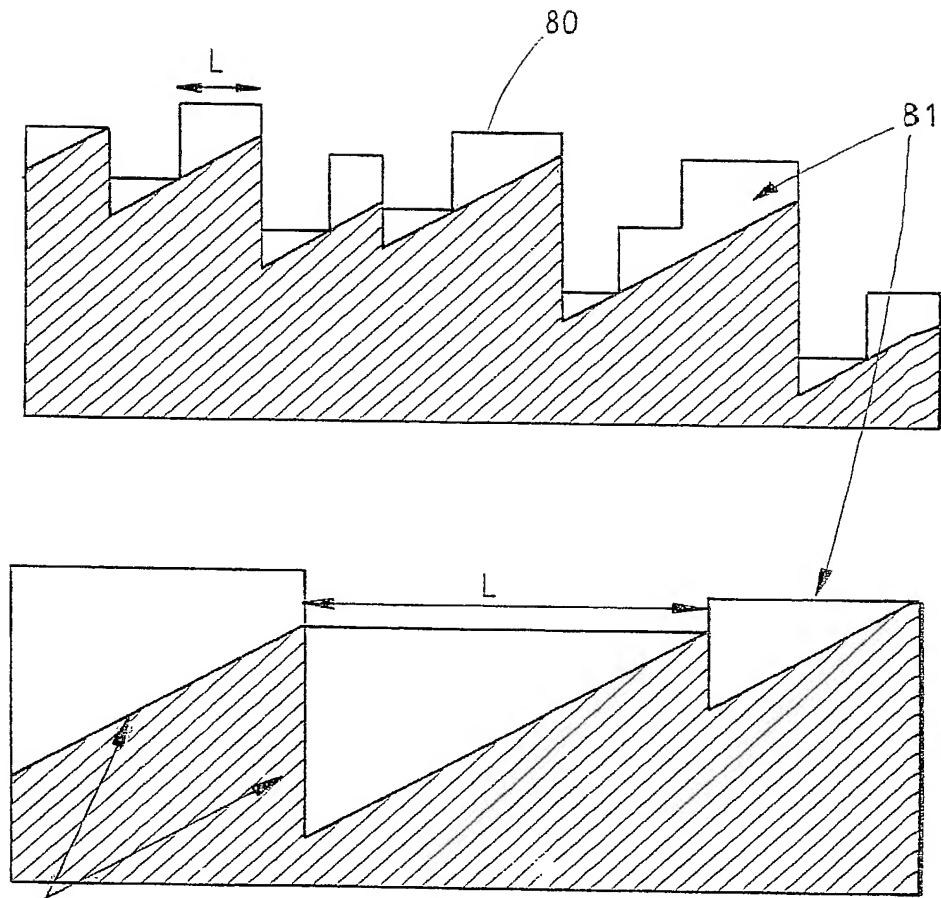
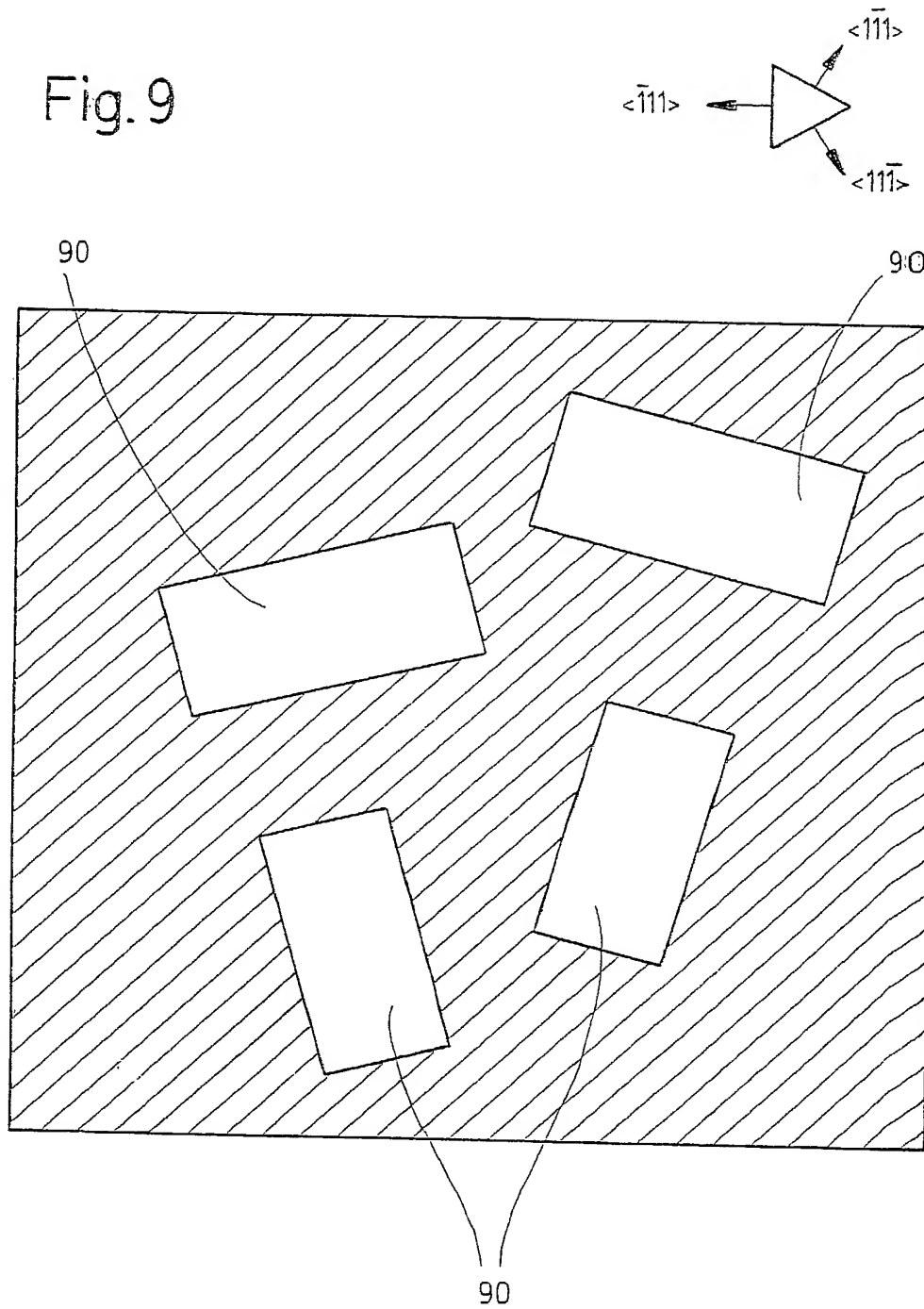


Fig. 9



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